

## CLAIMS

What is claimed is:

- 1 1. An interface transmitter coupled among a plurality of network  
2 elements of at least one network, wherein a plurality of data frames of a first  
3 type are received from at least one processor and stored in at least one  
4 random access memory (RAM), wherein data is read from the at least one  
5 RAM to at least one data serializer in response to a plurality of signals  
6 received from the at least one processor and over at least one backplane  
7 network, wherein a plurality of data frames of a second type corresponding  
8 to the plurality of data frames of a first type are generated and serially  
9 transferred among the plurality of network elements using the at least one  
10 backplane network.
- 1 2. The interface transmitter of claim 1, wherein the at least one data  
2 frame of a second type comprises switching event information of the  
3 plurality of network elements.
- 1 3. The interface transmitter of claim 1, wherein the at least one  
2 backplane network is further coupled to transfer the at least one data frame  
3 of a second type among at least one receiver and the at least one processor,  
4 wherein compare operations are performed among prespecified data frames  
5 of a second type at prespecified intervals, wherein at least one interrupt  
6 signal is generated in response to data changes determined by the compare  
7 operations, wherein protection switching is controlled in the at least one  
8 network by the at least one processor in response to the at least one interrupt  
9 signal.
- 1 4. The interface transmitter of claim 3, wherein generating at least one  
2 interrupt signal comprises generating at least one unit interrupt signal in

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3 response to the data changes, generating at least one memory map in  
4 response to the at least one unit interrupt signal, and generating at least one  
5 massive interrupt signal in response to the at least one unit interrupt signal.

1 5. The interface transmitter of claim 1, wherein protection switching is  
2 controlled in the plurality of network elements by the at least one processor  
3 in response to the switching event information, wherein the at least one  
4 processor navigates among a plurality of memory locations using a plurality  
5 of memory maps in response to at least one interrupt signal, reads data from  
6 the plurality of memory locations relating to the switching event  
7 information, and evaluates the switching event information.

1 6. The interface transmitter of claim 1, wherein the at least one  
2 backplane network comprises a 16-channel bus.

1 7. The interface transmitter of claim 1, wherein the plurality of data  
2 frames of a first format correspond to a plurality of input channels among  
3 the plurality of network elements.

1 8. The interface transmitter of claim 1, wherein the at least one RAM  
2 comprises a plurality of memory areas distributed among the plurality of  
3 network elements.

1 9. The interface transmitter of claim 1, wherein the at least one RAM  
2 comprises at least one dual port RAM.

1 10. The interface transmitter of claim 1, wherein the storing comprises  
2 multiplexing the plurality of data frames of a first type into at least one  
3 field-programmable gate array (FPGA).

1 11. The interface transmitter of claim 1, wherein the at least one data  
2 frame of a second type comprises approximately 67.5 bytes comprising

3 status bytes and Synchronous Optical Network (SONET) bytes including  
4 K1, K2, E1, and F1 bytes transferred as a serial bit stream at a rate of  
5 approximately 4.32 megahertz.

1 12. The interface transmitter of claim 1, wherein the at least one  
2 processor includes a plurality of processors distributed among the plurality  
3 of network elements.

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